What is claimed is:

1. A method for abstracting a precharged latch, comprising:

accessing a logic level representation of a structure, said logic level representation comprising a data node, and a clock node for receiving a clock signal, said clock signal having multiple phases;

deriving a first resultant cofactor based upon said logic level representation and a first phase of said clock signal;

determining whether said first resultant cofactor indicates: (1) a first node of said logic level representation experiencing a precharge; and (2) a second node of said logic level representation maintaining a previous logic value;

in response to an affirmative determination, concluding that said second node is a precharged latch candidate;

deriving a second resultant cofactor based upon said logic level representation and a second phase of said clock signal;

determining whether said second resultant cofactor is devoid of a feedback loop; and

in response to an affirmative determination, abstracting said structure as a precharged latch.

2. The method of claim 1, wherein deriving said first resultant cofactor comprises:

performing cofactor computation on said logic level representation while restricting said clock signal to a particular logic value.

3. The method of claim 2, wherein deriving said second resultant cofactor comprises:

performing cofactor computation on said logic level representation while restricting said clock signal to another logic value which is different from said particular logic value.

4. The method of claim 2, wherein said logic level representation further comprises a charge storage delay coupled to said first node, and wherein deriving said second resultant cofactor comprises:

propagating said precharge experienced by said first node through said charge storage delay; and

thereafter performing cofactor computation on said logic level representation while restricting said clock signal to another logic value which is different from said particular logic value.

5. The method of claim 1, wherein determining whether said first resultant cofactor indicates that said second node is maintaining a previous logic value comprises:

determining whether said second node is part of a feedback loop.

6. The method of claim 1, wherein said logic level representation further comprises a feedback loop delay, and wherein determining whether said first resultant cofactor indicates that said second node is maintaining a previous logic value comprises:

determining whether said second node is coupled to said feedback loop delay.

7. The method of claim 1, further comprising:

in response to a determination that said first resultant cofactor indicates either: (1) that said first node of said logic level representation does not experience a precharge; or (2) that said second node of said logic level representation does not maintain a previous logic value, concluding that said structure is not a precharged latch.

8. The method of claim 1, further comprising:

in response to a determination that said second resultant cofactor is not devoid of a feedback loop, concluding that said structure is not a precharged latch.

9. A computer readable medium, comprising:

instructions for causing one or more processors to access a logic level representation of a structure, said logic level representation comprising a data node, and a clock node for receiving a clock signal, said clock signal having multiple phases;

instructions for causing one or more processors to derive a first resultant cofactor based upon said logic level representation and a first phase of said clock signal;

instructions for causing one or more processors to determine whether said first resultant cofactor indicates: (1) a first node of said logic level representation experiencing a precharge; and (2) a second node of said logic level representation maintaining a previous logic value;

instructions for causing one or more processors to conclude, in response to an affirmative determination, that said second node is a precharged latch candidate;

instructions for causing one or more processors to derive a second resultant cofactor based upon said logic level representation and a second phase of said clock signal;

instructions for causing one or more processors to determine whether said second resultant cofactor is devoid of a feedback loop; and

instructions for causing one or more processors to abstract, in response to an affirmative determination, said structure as a precharged latch.

10. The computer readable medium of claim 9, wherein the instructions for causing one or more processors to derive said first resultant cofactor comprises:

instructions for causing one or more processors to perform cofactor computation on said logic level representation while restricting said clock signal to a particular logic value.

11. The computer readable medium of claim 10, wherein the instructions for causing one or more processors to derive said second resultant cofactor comprises:

instructions for causing one or more processors to perform cofactor computation on said logic level representation while restricting said clock signal to another logic value which is different from said particular logic value.

12. The computer readable medium of claim 10, wherein said logic level representation further comprises a charge storage delay coupled to said first node, and wherein the instructions for causing one or more processors to derive said second resultant cofactor comprises:

instructions for causing one or more processors to propagate said precharge experienced by said first node through said charge storage delay; and

instructions for causing one or more processors to thereafter perform cofactor computation on said logic level representation while restricting said clock signal to another logic value which is different from said particular logic value.

13. The computer readable medium of claim 9, wherein the instructions for causing one or more processors to determine whether said first resultant cofactor indicates that said second node is maintaining a previous logic value comprises:

instructions for causing one or more processors to determine whether said second node is part of a feedback loop.

14. The computer readable medium of claim 9, wherein said logic level representation further comprises a feedback loop delay, and wherein the instructions for causing one or more processors to determine whether said first resultant cofactor indicates that said second node is maintaining a previous logic value comprises:

instructions for causing one or more processors to determine whether said second node is coupled to said feedback loop delay.

15. The computer readable medium of claim 9, further comprising:

instructions for causing one or more processors to conclude, in response to a determination that said first resultant cofactor indicates either: (1) that said first node of said logic level representation does not experience a precharge; or (2) that said second node of said logic level representation does not maintain a previous logic value, that said structure is not a precharged latch.

16. The computer readable medium of claim 9, further comprising:

instructions for causing one or more processors to conclude, in response to a determination that said second resultant cofactor is not devoid of a feedback loop, that said structure is not a precharged latch.

17. An apparatus for abstracting a precharged latch, comprising:

a mechanism for accessing a logic level representation of a structure, said logic level representation comprising a data node, and a clock node for receiving a clock signal, said clock signal having multiple phases;

a mechanism for deriving a first resultant cofactor based upon said logic level representation and a first phase of said clock signal;

a mechanism for determining whether said first resultant cofactor indicates: (1) a first node of said logic level representation experiencing a precharge; and (2) a second node of said logic level representation maintaining a previous logic value;

a mechanism for concluding, in response to an affirmative determination, that said second node is a precharged latch candidate;

a mechanism for deriving a second resultant cofactor based upon said logic level representation and a second phase of said clock signal;

a mechanism for determining whether said second resultant cofactor is devoid of a feedback loop; and

a mechanism for abstracting, in response to an affirmative determination, said structure as a precharged latch.

18. The apparatus of claim 17, wherein the mechanism for deriving said first resultant cofactor comprises:

a mechanism for performing cofactor computation on said logic level representation while restricting said clock signal to a particular logic value.

19. The apparatus of claim 18, wherein the mechanism for deriving said second resultant cofactor comprises:

a mechanism for performing cofactor computation on said logic level representation while restricting said clock signal to another logic value which is different from said particular logic value.

20. The apparatus of claim 18, wherein said logic level representation further comprises a charge storage delay coupled to said first node, and wherein the mechanism for deriving said second resultant cofactor comprises:

a mechanism for propagating said precharge experienced by said first node through said charge storage delay; and

a mechanism for thereafter performing cofactor computation on said logic level representation while restricting said clock signal to another logic value which is different from said particular logic value.

21. The apparatus of claim 17, wherein the mechanism for determining whether said first resultant cofactor indicates that said second node is maintaining a previous logic value comprises:

a mechanism for determining whether said second node is part of a feedback loop.

22. The apparatus of claim 17, wherein said logic level representation further comprises a feedback loop delay, and wherein the mechanism for determining whether said first resultant cofactor indicates that said second node is maintaining a previous logic value comprises:

a mechanism for determining whether said second node is coupled to said feedback loop delay.

23. The apparatus of claim 17, further comprising:

a mechanism for concluding, in response to a determination that said first resultant cofactor indicates either: (1) that said first node of said logic level representation does not experience a precharge; or (2) that said second node of said logic level representation does not maintain a previous logic value, that said structure is not a precharged latch.

24. The apparatus of claim 17, further comprising:

a mechanism for concluding, in response to a determination that said second resultant cofactor is not devoid of a feedback loop, that said structure is not a precharged latch.

25. A method for abstracting a precharged flip-flop, comprising:

accessing a logic level representation of a structure, said logic level representation comprising a data node, and a clock node for receiving a clock signal, said clock signal having multiple phases;

deriving a first resultant cofactor based upon said logic level representation and a first phase of said clock signal;

determining whether said first resultant cofactor indicates: (1) a first node of said logic level representation experiencing a first precharge; (2) a second node of said logic level representation experiencing a second precharge; and (3) a third node of said logic level representation maintaining a previous logic value;

in response to an affirmative determination, concluding that said third node is a precharged flip-flop candidate;

deriving a second resultant cofactor based upon said logic level representation and a second phase of said clock signal;

determining whether said second resultant cofactor is devoid of a feedback loop;

in response to an affirmative determination, concluding that said third node is still a precharged flip-flop candidate;

determining, based upon said logic level representation, said second phase of said clock signal, and an assumption that said first and second nodes have complementary logic values, whether logic values taken on by said third node are independent of logic values taken on by said data node; and

in response to an affirmative determination, abstracting said structure as a precharged flip-flop.

26. The method of claim 25, wherein deriving said first resultant cofactor comprises:

performing cofactor computation on said logic level representation while restricting said clock signal to a particular logic value.

27. The method of claim 26, wherein deriving said second resultant cofactor comprises:

performing cofactor computation on said logic level representation while restricting said clock signal to another logic value which is different from said particular logic value.

28. The method of claim 26, wherein said logic level representation further comprises a first delay coupled to said first node, and a second delay coupled to said second node, and wherein deriving said second resultant cofactor comprises:

propagating said first precharge through said first delay, and said second precharge through said second delay; and

thereafter performing cofactor computation on said logic level representation while restricting said clock signal to another logic value which is different from said particular logic value.

29. The method of claim 28, wherein determining whether logic values taken on by said third node are independent of logic values taken on by said data node comprises:

propagating a logic 1 value from said first node through said first delay, and a logic 0 value from said second node through said second delay; and

thereafter performing cofactor computation on said logic level representation while restricting said clock signal to said another logic value to derive a third resultant cofactor.

30. The method of claim 29, wherein determining whether logic values taken on by said third node are independent of logic values taken on by said data node further comprises:

propagating a logic 0 value from said first node through said first delay, and a logic 1 value from said second node through said second delay; and

thereafter performing cofactor computation on said logic level representation while restricting said clock signal to said another logic value to derive a fourth resultant cofactor.

31. The method of claim 30, wherein determining whether logic values taken on by said third node are independent of logic values taken on by said data node further comprises:

determining whether said third and fourth resultant cofactors indicate that logic values taken on by said third node are independent of logic values taken on by said data node.

32. The method of claim 25, wherein determining whether said first resultant cofactor indicates that said third node is maintaining a previous logic value comprises:

determining whether said third node is part of a feedback loop.

33. The method of claim 25, wherein said logic level representation further comprises a feedback loop delay, and wherein determining whether said first resultant cofactor indicates that said third node is maintaining a previous logic value comprises:

determining whether said third node is coupled to said feedback loop delay.

34. The method of claim 25, further comprising:

in response to a determination that said first resultant cofactor indicates either: (1) that said first node of said logic level representation does not experience said first precharge; or (2) that said second node of said logic level representation does not experience said second precharge; or (3) that said third node of said logic level representation does not maintain a previous logic value, concluding that said structure is not a precharged flip-flop.

35. The method of claim 25, further comprising:

in response to a determination that said second resultant cofactor is not devoid of a feedback loop, concluding that said structure is not a precharged flip-flop.

36. The method of claim 25, further comprising:

in response to a determination that logic values taken on by said third node are not independent of logic values taken on by said data node when an assumption that said first and second nodes have complementary logic values is made, concluding that said structure is not a precharged flip-flop.

37. A computer readable medium, comprising:

instructions for causing one or more processors to access a logic level representation of a structure, said logic level representation comprising a data node, and a clock node for receiving a clock signal, said clock signal having multiple phases;

instructions for causing one or more processors to derive a first resultant cofactor based upon said logic level representation and a first phase of said clock signal;

instructions for causing one or more processors to determine whether said first resultant cofactor indicates: (1) a first node of said logic level representation experiencing a first precharge; (2) a second node of said logic level representation experiencing a second precharge; and (3) a third node of said logic level representation maintaining a previous logic value;

instructions for causing one or more processors to conclude, in response to an affirmative determination, that said third node is a precharged flip-flop candidate;

instructions for causing one or more processors to derive a second resultant cofactor based upon said logic level representation and a second phase of said clock signal;

instructions for causing one or more processors to determine whether said second resultant cofactor is devoid of a feedback loop;

instructions for causing one or more processors to conclude, in response to an affirmative determination, that said third node is still a precharged flip-flop candidate;

instructions for causing one or more processors to determine, base d upon said logic level representation, said second phase of said clock signal, and an assumption that said first and second nodes have complementary logic values, whether logic values taken on by said third node are independent of logic values taken on by said data node; and

instructions for causing one or more processors to abstract, in response to an affirmative determination, said structure as a precharged flip-flop.

38. The computer readable medium of claim 37, wherein the instructions for causing one or more processors to derive said first resultant cofactor comprises:

instructions for causing one or more processors to perform cofactor computation on said logic level representation while restricting said clock signal to a particular logic value.

39. The computer readable medium of claim 38, wherein the instructions for causing one or more processors to derive said second resultant cofactor comprises:

instructions for causing one or more processors to perform cofactor computation on said logic level representation while restricting said clock signal to another logic value which is different from said particular logic value.

40. The computer readable medium of claim 38, wherein said logic level representation further comprises a first delay coupled to said first node, and a second delay coupled to said second node, and wherein the instructions for causing one or more processors to derive said second resultant cofactor comprises:

instructions for causing one or more processors to propagate said first precharge through said first delay, and said second precharge through said second delay; and

instructions for causing one or more processors to thereafter perform cofactor computation on said logic level representation while restricting said clock signal to another logic value which is different from said particular logic value.

41. The computer readable medium of claim 40, wherein the instructions for causing one or more processors to determine whether logic values taken on by said third node are independent of logic values taken on by said data node comprises:

instructions for causing one or more processors to propagate a logic 1 value from said first node through said first delay, and a logic 0 value from said second node through said second delay; and

instructions for causing one or more processors to thereafter perform cofactor computation on said logic level representation while restricting said clock signal to said another logic value to derive a third resultant cofactor.

42. The computer readable medium of claim 41, wherein the instructions for causing one or more processors to determine whether logic values taken on by said third node are independent of logic values taken on by said data node further comprises:

instructions for causing one or more processors to propagate a logic 0 value from said first node through said first delay, and a logic 1 value from said second node through said second delay; and

instructions for causing one or more processors to thereafter perform cofactor computation on said logic level representation while restricting said clock signal to said another logic value to derive a fourth resultant cofactor.

43. The computer readable medium of claim 42, wherein the instructions for causing one or more processors to determine whether logic values taken on by said third node are independent of logic values taken on by said data node further comprises:

instructions for causing one or more processors to determine whether said third and fourth resultant cofactors indicate that logic values taken on by said third node are independent of logic values taken on by said data node.

44. The computer readable medium of claim 37, wherein the instructions for causing one or more processors to determine whether said first resultant cofactor indicates that said third node is maintaining a previous logic value comprises:

instructions for causing one or more processors to determine whether said third node is part of a feedback loop.

45. The computer readable medium of claim 37, wherein said logic level representation further comprises a feedback loop delay, and wherein the instructions for causing one or more processors to determine whether said first resultant cofactor indicates that said third node is maintaining a previous logic value comprises:

instructions for causing one or more processors to determine whether said third node is coupled to said feedback loop delay.

46. The computer readable medium of claim 37, further comprising:

instructions for causing one or more processors to conclude, in response to a determination that said first resultant cofactor indicates either: (1) that said first node of said logic level representation does not experience said first precharge; or (2) that said second node of said logic level representation does not experience said second precharge; or (3) that said third node of said logic level representation does not maintain a previous logic value, that said structure is not a precharged flip-flop.

47. The computer readable medium of claim 37, further comprising:

instructions for causing one or more processors to conclude, in response to a determination that said second resultant cofactor is not devoid of a feedback loop, that said structure is not a precharged flip-flop.

48. The computer readable medium of claim 37, further comprising:

instructions for causing one or more processors to conclude, in response to a determination that logic values taken on by said third node are not independent of logic values taken on by said data node when an assumption that said first and second nodes have complementary logic values is made, that said structure is not a precharged flip-flop.

49. An apparatus for abstracting a precharged flip-flop, comprising:

a mechanism for accessing a logic level representation of a structure, said logic level representation comprising a data node, and a clock node for receiving a clock signal, said clock signal having multiple phases;

a mechanism for deriving a first resultant cofactor based upon said logic level representation and a first phase of said clock signal;

a mechanism for determining whether said first resultant cofactor indicates: (1) a first node of said logic level representation experiencing a first precharge; (2) a second node of said logic level representation experiencing a second precharge; and (3) a third node of said logic level representation maintaining a previous logic value;

a mechanism for concluding, in response to an affirmative determination, that said third node is a precharged flip-flop candidate;

a mechanism for deriving a second resultant cofactor based upon said logic level representation and a second phase of said clock signal;

a mechanism for determining whether said second resultant cofactor is devoid of a feedback loop;

a mechanism for concluding, in response to an affirmative determination, that said third node is still a precharged flip-flop candidate;

a mechanism for determining, based upon said logic level representation, said second phase of said clock signal, and an assumption that said first and second nodes have complementary logic values, whether logic values taken on by said third node are independent of logic values taken on by said data node; and

a mechanism for abstracting, in response to an affirmative determination, said structure as a precharged flip-flop.

50. The apparatus of claim 49, wherein the mechanism for deriving said first resultant cofactor comprises:

a mechanism for performing cofactor computation on said logic level representation while restricting said clock signal to a particular logic value.

51. The apparatus of claim 50, wherein the mechanism for deriving said second resultant cofactor comprises:

a mechanism for performing cofactor computation on said logic level representation while restricting said clock signal to another logic value which is different from said particular logic value.

52. The apparatus of claim 50, wherein said logic level representation further comprises a first delay coupled to said first node, and a second delay coupled to said second node, and wherein the mechanism for deriving said second resultant cofactor comprises:

a mechanism for propagating said first precharge through said first delay, and said second precharge through said second delay; and

a mechanism for thereafter performing cofactor computation on said logic level representation while restricting said clock signal to another logic value which is different from said particular logic value.

53. The apparatus of claim 52, wherein the mechanism for determining whether logic values taken on by said third node are independent of logic values taken on by said data node comprises:

a mechanism for propagating a logic 1 value from said first node through said first delay, and a logic 0 value from said second node through said second delay; and

a mechanism for thereafter performing cofactor computation on said logic level representation while restricting said clock signal to said another logic value to derive a third resultant cofactor.

54. The apparatus of claim 53, wherein the mechanism for determining whether logic values taken on by said third node are independent of logic values taken on by said data node further comprises:

a mechanism for propagating a logic 0 value from said first node through said first delay, and a logic 1 value from said second node through said second delay; and

a mechanism for thereafter performing cofactor computation on said logic level representation while restricting said clock signal to said another logic value to derive a fourth resultant cofactor.

55. The apparatus of claim 54, wherein the mechanism for determining whether logic values taken on by said third node are independent of logic values taken on by said data node further comprises:

a mechanism for determining whether said third and fourth resultant cofactors indicate that logic values taken on by said third node are independent of logic values taken on by said data node.

56. The apparatus of claim 49, wherein the mechanism for determining whether said first resultant cofactor indicates that said third node is maintaining a previous logic value comprises:

a mechanism for determining whether said third node is part of a feedback loop.

57. The apparatus of claim 49, wherein said logic level representation further comprises a feedback loop delay, and wherein the mechanism for determining whether said first resultant cofactor indicates that said third node is maintaining a previous logic value comprises:

a mechanism for determining whether said third node is coupled to said feedback loop delay.

58. The apparatus of claim 49, further comprising:

a mechanism for concluding, in response to a determination that said first resultant cofactor indicates either: (1) that said first node of said logic level representation does not experience said first precharge; or (2) that said second node of said logic level representation does not experience said second precharge; or (3) that said third node of said logic level representation does not maintain a previous logic value, that said structure is not a precharged flip-flop.

59. The apparatus of claim 49, further comprising:

a mechanism for concluding, in response to a determination that said second resultant cofactor is not devoid of a feedback loop, that said structure is not a precharged flip-flop.

60. The apparatus of claim 49, further comprising:

a mechanism for concluding, in response to a determination that logic values taken on by said third node are not independent of logic values taken on by said data node when an assumption that said first and second nodes have complementary logic values is made, that said structure is not a precharged flip-flop.